CLAIMS

What is claimed is:

1. A memory modeling circuit with fault toleration, comprising:

a compare circuit, comparing data stored in the same address of a plurality of memories; and

a control circuit coupled to said plurality of memories, wherein said control circuit controls said data to be read or written from/to said plurality of memories.

2. The circuit according to claim 1, further comprising:

a test circuit, receiving said data and the reading data generated by said compare circuit to generate a testing result.

3. The circuit according to claim 2, wherein said test circuit further comprises a plurality of sub-test circuits with the same circuit design.

4. The circuit according to claim 3, wherein said testing result gets an error code and then a faulty memory or a faulty sub-test circuit can be identified according to said error code.

5. The circuit according to claim 1, wherein said plurality of memories are the same type of memory.

6. The circuit according to claim 5, wherein said memory is synchronous dynamic random access memory (SDRAM).

7. The circuit according to claim 1, wherein said compare circuit further comprises a plurality of sub-compare circuits with the same circuit design.

8. The circuit according to claim 1, wherein said control circuit stops receiving the data sent from said compare circuit until said control circuit enters the reading mode while said control circuit is in the writing mode.

9. The circuit according to claim 1, wherein said control circuit makes said compare circuit stop writing the data to said plurality of memories until said control circuit enters the writing mode while said control circuit is in the reading mode.

10. A memory modeling circuit with fault toleration, comprising:

a compare circuit receiving data stored in the same address of a plurality of memories and comparing the data with each other;

a control circuit connecting said plurality of memories, wherein said control circuit enters a writing mode and writes data to the same

address of said plurality of memories, and said control circuit enters a reading mode to load data generated by said compare circuit; and

a test circuit receiving the data stored in the same address of said plurality of memories and the data generated by said compare circuit to generate a testing result.

11. The circuit according to claim 10, wherein said test circuit further comprises a plurality of sub-test circuits with the same circuit design.

12. The circuit according to claim 11, wherein said testing result can identify a faulty memory or a faulty sub-test circuit.

13. The circuit according to claim 10, wherein said compare circuit further comprises a plurality of sub-compare circuits with the same circuit design.

14. The circuit according to claim 10, wherein said testing result gets an error code and then an engineer knows the fault part according to different error code combinations and repair said fault part to keep the reliability.

15. The circuit according to claim 10, wherein said plurality of memories are the same type of memory.

16. The circuit according to claim 15, wherein said memory is synchronous dynamic random access memory (SDRAM).

17. The circuit according to claim 10, wherein said control circuit stops receiving data sent from said compare circuit until said control circuit enters the reading mode while said control circuit is in the writing mode.

18. The circuit according to claim 10, wherein said control circuit makes said compare circuit stop writing data to said plurality of memories until said control circuit enters the writing mode while said control circuit is in the reading mode.